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## Ultra-thin silicon on sapphire for high-density AMLCD drivers

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### ABSTRACT

Single-crystal ultra-thin ( $< 100$  nm) silicon on sapphire (UTSOS) has been fabricated using solid-phase epitaxy and regrowth techniques to produce a high quality semiconductor material on a transparent substrate ideal for active-matrix liquid crystal display (AMLCD) applications. MOS devices fabricated in this material have lower leakages, smaller thresholds, and higher transconductances than those fabricated in conventional unimproved SOS.

The low mobility and poor quality of amorphous and polysilicon materials currently being used for AMLCD's severely limit the performance of integrated drivers. UTSOS device characteristics and projected shift register performances are superior to those obtained by polysilicon and amorphous silicon processes. The higher speed of UTSOS devices allows one to exploit the advantages of ferroelectric liquid crystal (FLC) materials on a transparent substrate whose previous demonstrations were limited to bulk silicon devices. The higher speeds of the FLC's allow the use of time multiplexed gray levels and color generation with the corresponding increase in effective pixel density. Preliminary layouts and SPICE simulations for a 1000 X 1000 array of FLC pixels are described.

Improvements obtained using UTSOS offer a viable alternative for AMLCD systems. Predicted aperture ratios and pixel sizes are applicable for efficient, small-size, high-density displays with integrated drive and signal processing circuitry.

### 1. INTRODUCTION

There is an increasing demand for small-size high-density displays. Applications include projection systems, head-mounted systems and camcorder viewfinders. The mainstream approach to active-matrix liquid-crystal displays (AMLCD's) is to fabricate the active-matrix elements in thin layers of amorphous silicon or polysilicon deposited on glass or quartz substrates. In order to realize small-size high-density displays, it is highly advantageous to integrate the drive circuitry onto the same substrate as the active matrix. Integration of the drive circuitry will

reduce the cost, size, and increase the performance of the display. The mobility and poor quality of amorphous and polysilicon materials severely limit the performance of the drivers integrated with these AMLCD technologies. The use of integrated single-crystal silicon drivers has been proposed to resolve this problem<sup>1-3</sup>. This paper looks at the feasibility of applying improved silicon-on-sapphire technology for this same purpose.

## 2. BACKGROUND

### 2.1 UTSOS

Silicon on sapphire (SOS) is the most mature silicon on insulator technology. The primary market for SOS has been for military and aerospace applications which require radiation hardness. Very large scale integration (VLSI) commercial parts have been available for several years.

Because of its transparent substrate, SOS was used to fabricate some of the first demonstrations of AMLCD's<sup>4</sup>. However, the unavailability of large substrates has precluded its use for large flat panel displays. While SOS is recognized as an ideal material to fabricate the display drive circuits for a small-sized display, conventional SOS devices have leakage currents too high to utilize them as switching elements in active-matrix displays<sup>5</sup>.

Conventional SOS processing uses an epitaxially grown, single crystal silicon film thickness of about 300 nm. Thinner silicon films are advantageous because they further reduce parasitic capacitances, reduce short channel effects, allow for fully depleted operation (where the depletion depth  $< t_{Si}$ , the silicon thickness), and the absorption of light by the active silicon films is reduced. Thinner silicon films are usually avoided because of the large number of defects near the as-grown silicon/sapphire interface. Using solid-phase epitaxy, we have significantly improved the crystal quality of SOS at the silicon/sapphire interface<sup>6</sup>. This allows us to fabricate circuitry in ultra-thin ( $< 100$  nm) silicon on sapphire (UTSOS). Metal-oxide-semiconductor (MOS) devices fabricated in this material have lower leakages, smaller thresholds, and higher transconductances than those fabricated in unimproved SOS. This is due to the increased mobility and the creation of fully depleted films. Fully depleted operation has been shown to improve transistor performance by steepening the sub-threshold slope<sup>7</sup> of MOSFET's and by reducing the "kink" effect due to a floating substrate<sup>8</sup>. Very high performance devices have been made in these films using 0.5 micron gate lengths with resulting unity-gain frequencies,  $f_t$ 's, of 20 Ghz<sup>9</sup>.

### 2.2 FLC's

Ferroelectric liquid crystals (FLC's) have a combination of properties and characteristics that uniquely qualify them for integrated opto-electronic devices<sup>10</sup>. Their strong optical interaction permits thin layers to completely modulate light, while their low-voltage switching keeps power dissipation low enough for dense packing, and allows driving directly by ordinary complementary-metal-oxide-semiconductor (CMOS) circuits, a technology amenable to very large scale integration. The inert, liquid nature of FLC's allows them to be readily formed on almost any smooth substrate. Individual modulator elements (pixels) are simply defined by patterned electrodes that can be fabricated by standard photolithographic techniques. Thus, high-quality optically functional layers may be directly formed on and driven by ordinary silicon-based integrated circuits.

The FLC device in its simplest form is binary. Unlike nematic liquid crystals whose gray

scale is generated by a number of stable intermediate transmission states, FLC's use a variety of techniques to achieve suitable gray scales such as spatial, temporal, threshold, charge-controlled, and field-variation techniques. A comprehensive review of gray scale in FLC's has been made by Hartmann<sup>11</sup>. In their ON state, pixels transmit a broad spectrum of incident white light, imparting no color of their own. In their OFF state, the pixels uniformly block light of all wavelengths, with achievable contrast ratios over 1000:1 and 0.1% settling times of a few hundred microseconds. These characteristics permit generation of high-fidelity gray-scale and full-color images. Exploiting the high speed of CMOS devices in UTSOS, gray scales can be achieved straight forwardly by temporal duty-cycle variation. This approach generates analog representations by precise variation in the time domain, a strength of digital electronic systems.

Color can be generated by a variety of techniques. Images of separate arrays for each color can be combined on dichroic beam splitters. This technique is especially appropriate to projection displays. Alternately, color can be achieved by field sequential techniques. A single image-generating element can be sequentially illuminated with red, green, and blue light to build up a full-color image. This technique is especially appropriate to miniature displays and to color printing.

### 3. DESIGN ISSUES

Table I shows UTSOS device characteristics and projected shift register performance compared to a low and high temperature polysilicon processes and an amorphous silicon process. Note the low thresholds that can be obtained with the UTSOS and the factor of ~ 4 improvement in n-channel mobility (p-channel mobility in UTSOS is ~ 200 cm<sup>2</sup>/V-s). The high quality, single crystal UTSOS films allow the use of thin, reliable gate oxides and short (1.0 micron) gate lengths, leading to high speed (> 100 Mhz) circuits.

| Table I. Comparison of MOS Technologies for Active Matrix Displays <sup>12</sup> |                     |                         |                        |                                |
|--|---------------------|-------------------------|------------------------|--------------------------------|
|  | Poly-TFT<br>HT CMOS | Poly-TFT<br>MT-<br>CMOS | $\alpha$ -Si:H<br>NMOS | CMOS<br>UTSOS                  |
| 1. Substrate   | fused quartz        | hard glass              | hard glass             | Al <sub>2</sub> O <sub>3</sub> |
| 2. Max. process temp.  | ~1000°C             | 600°C                   | 300°C                  | 1000°C                         |
| 3. Thresholds (Volts) (n-chnl)   | 2.0                 | 2.0                     | 1.5                    | 0.5                            |
| 4. Mobilities (cm <sup>2</sup> /Vs) (n-chnl)                                     | 100                 | 40                      | 0.75                   | 380                            |
| 5. Shift Register  | 20 Mhz<br>@15V      | 5 Mhz<br>@15V           | 0.1 Mhz<br>@15V        | >100Mhz<br>@5V                 |

The high speed of UTSOS allows one to exploit the advantages of ferroelectric liquid crystal (FLC) materials on a transparent substrate. Previous demonstrations were limited to bulk silicon

devices<sup>1,2</sup>. The higher speeds of the FLC's allow the use of time multiplexed gray levels and color generation with the corresponding increase in effective pixel density.

### 3.1 Pixel layout

Figure 1 shows a preliminary layout of a 12 X 12  $\mu\text{m}$  pixel using current NRaD design rules. Polysilicon row-select lines run horizontally and aluminum data lines run vertically down each column. The dotted lines show the row and column lines for the adjacent pixels. An optional

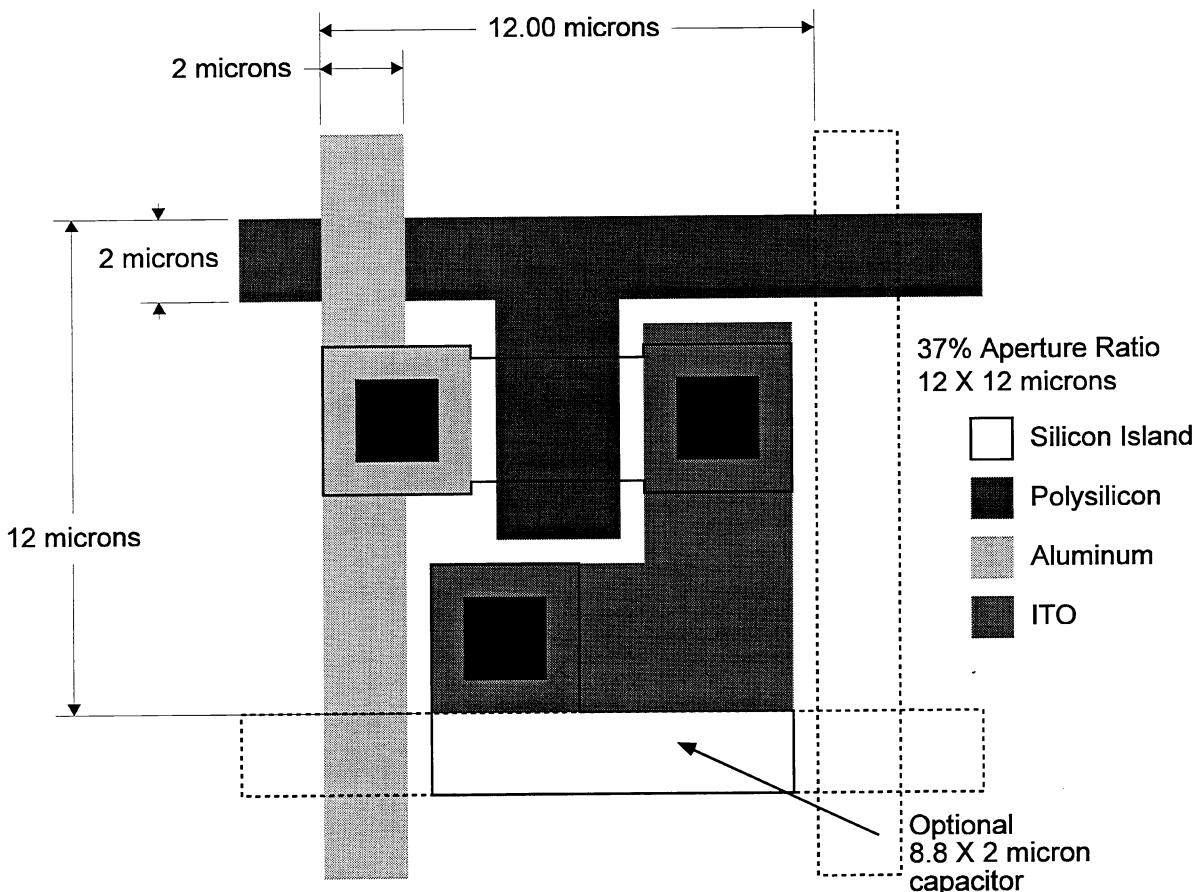


Figure 1. Proposed Pixel Layout for UTSOS AMLCD

storage capacitor formed between a silicon island and the adjacent row's polysilicon line is shown at the bottom of the pixel. This storage capacitor can be used to increase the decay time of the stored charge. The transistor element has dimensions of  $w = l = 3 \mu\text{m}$ . Calculated aperture ratios for other pixel sizes based on this layout are compared with other reported pixel sizes and aperture ratios in Table II. The aperture ratio (37%) was calculated by taking the area of the indium tin oxide (ITO) electrode divided by the total pixel area. A correction was made to account for absorption of light in the portions of silicon that lay under the ITO. Since the silicon films are very thin ( $0.1 \mu\text{m}$ ) this absorption is small (3.8%).

| TABLE II. COMPARISON OF PIXEL APERTURE RATIOS |                            |      |                    |
|---|----------------------------|------|--------------------|
|   | Pixel Dimensions (microns) |      | Aperture Ratio     |
|   | UTSOS                      | 10.0 |                    |
| 15.0  |                            | 15.0 | 0.52               |
| 20.0  |                            | 20.0 | 0.67               |
| 25.0  |                            | 25.0 | 0.75               |
| Polysilicon                                   | 29.0                       | 24.0 | 0.23 <sup>13</sup> |
|   | 34.0                       | 46.0 | 0.27 <sup>14</sup> |
|   | 21.5                       | 38   | 0.30 <sup>15</sup> |
|   | 45                         | 57   | 0.70 <sup>16</sup> |

### 3.2 Simulations

Figure 2 shows the equivalent circuit used to model the pixel element shown in Figure 1. PSPICE<sup>17</sup> was used to simulate the pixel element as it is would be used in a 1000 X 1000 array. CS is the parallel combination of the source capacitances of 1000 MOSFET's and is seen to be very small due to the small junction area of the source and drain. Rmetal and Rpoly are the resistances of the aluminum metal line and the polycide line, respectively. CG is the lumped gate capacitances of 1000 transistors with a 9  $\mu\text{m}^2$  gate area per pixel and is relatively high due to the thin (25 nm) oxide thickness used. C1 is the capacitance of a 58  $\mu\text{m}^2$  ferroelectric liquid crystal capacitor. V1 is the voltage on the other plate of the ferroelectric capacitor and is set at 7 volts for this simulation. Cb is included so that the substrate node does not float in PSPICE but instead tracks the potential of the source. Figure 3 shows measured output characteristics of the

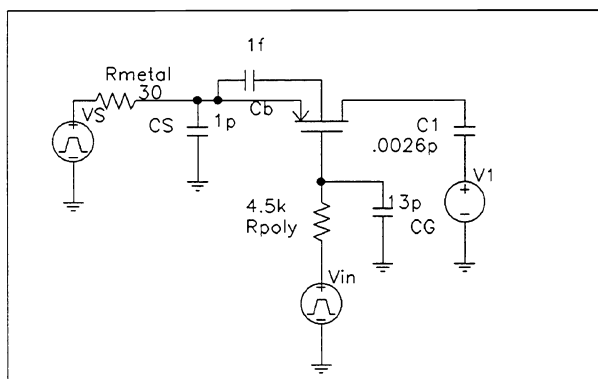


Figure 2. Schematic of Pixel Element Including Drive Line Capacitance and Resistance

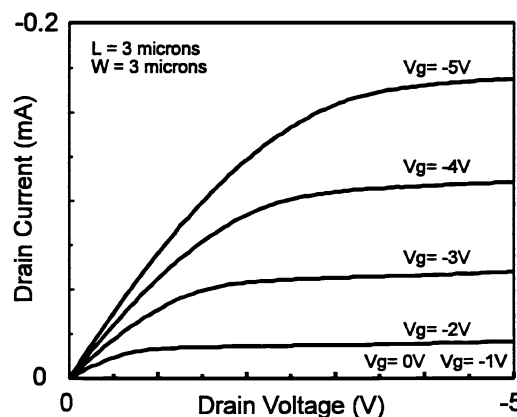


Figure 3. Output Characteristics of UTSOS p-MOS Transistor Used in this Simulation

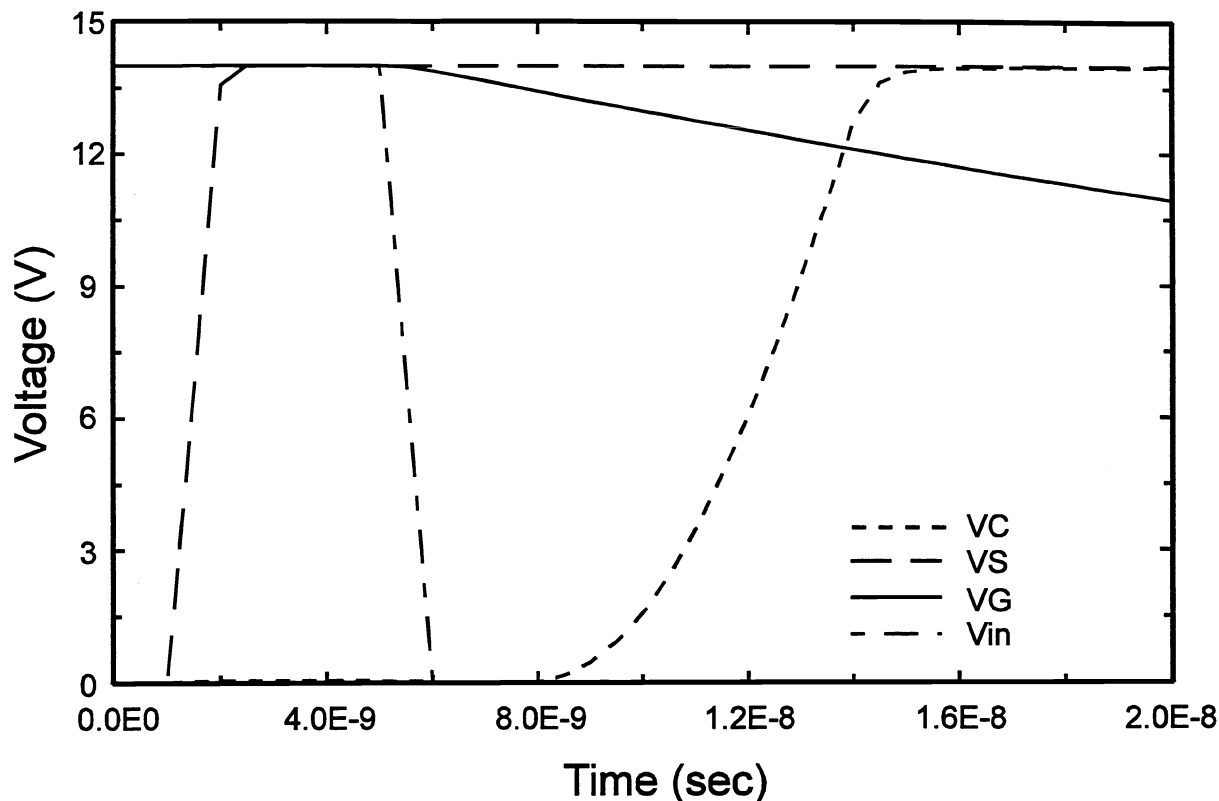


Figure 4. Simulated Voltage Transients for the Pixel Circuit

UTSOS p-channel MOSFET used to model the active-matrix switching element. Figure 4 depicts the simulated voltage transients for the pixel circuitry. VS is first switched from 0 to 14 volts to simulate setting the pixel's column voltage high. Vin is then dropped from 14 to 0 volts to simulate accessing of the pixel's row. VG, the voltage on the gate of the transistor, drops more slowly due to the capacitive loading of the 1000 gates which must be set in parallel and the resistive load of the 6.0 mm long polysilicon line. This is a worst case simulation in which the polysilicon drive line is driven from one end of the row line instead of in the middle or at both ends of the row line to access the farthest pixel. The voltage on the top plate of the pixel capacitor (VC) begins switching when VG drops below the switching transistor's threshold and is completely switched in 18 nanoseconds. This simulation shows that this design is capable of addressing the entire 1000 X 1000 pixel display in less than 20 microseconds. This illustrates the advantage of utilizing UTSOS with FLC's since the FLC's require this high rate of addressing in order to fully utilize them.

#### 4. COMPARISON TO OTHER SINGLE CRYSTAL SILICON APPROACHES

FLC's integrated with bulk silicon drivers have been demonstrated<sup>1,2</sup>. While these are attractive for their high speed, the lack of a transparent substrate limits their application to use in reflection mode. In another approach, the electronics are fabricated on a non-transparent recrystallized silicon on insulator material prepared by the isolated silicon epitaxy (ISE) process<sup>3</sup>.

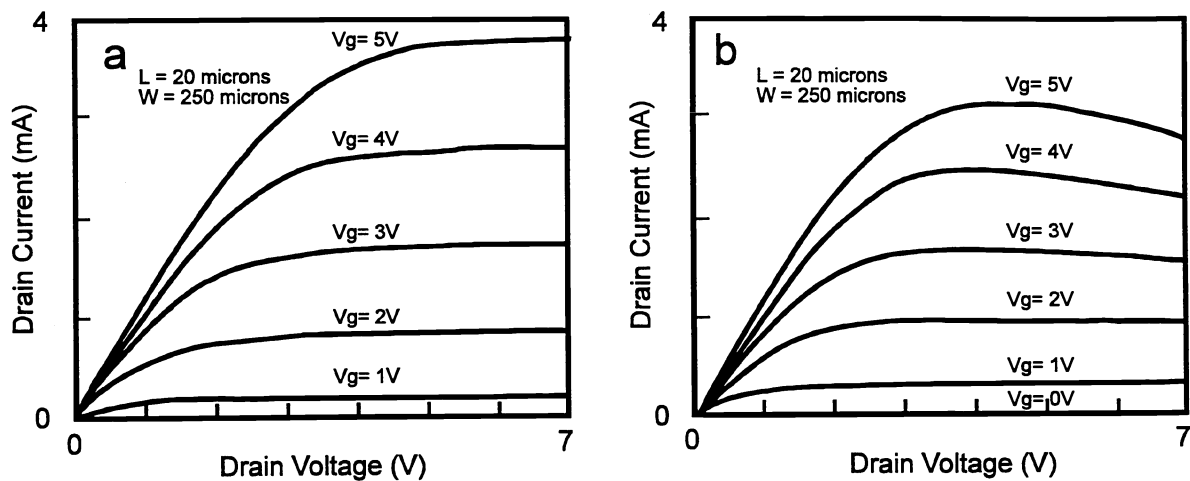


Figure 5. Output Characteristics for ISE Devices

- a) Before Transfer
- b) After Transfer

The display circuitry is then lifted off and transferred to a transparent substrate. The resulting circuit is then packaged in the standard manner to form the AMLCD. The UTSOS approach offers a significant advantage in that the electronics are fabricated directly on a transparent substrate. This eliminates the transfer process. Like the ISE process, UTSOS is compatible with standard silicon processing equipment. In addition, the UTSOS devices operate in a thinner (0.1 versus 0.3  $\mu\text{m}$ ) silicon layer. They are therefore fully depleted and do not require body ties. This will also be important for projection applications since the thinner silicon absorbs less light and the devices will have lower light-induced leakage currents. Figure 5 shows families of curves for the ISE devices both before and after transfer to the glass substrate<sup>18</sup>. Note the decrease in current in the saturation region after transfer. This phenomenon is known as self heating and comes about because of the poor thermal conductivity of the glass substrate<sup>19</sup>. Figure 6 shows the corresponding set of curves measured off a UTSOS device. The thermal conductivity of sapphire is much higher than glass and therefore the UTSOS devices do not have this problem.

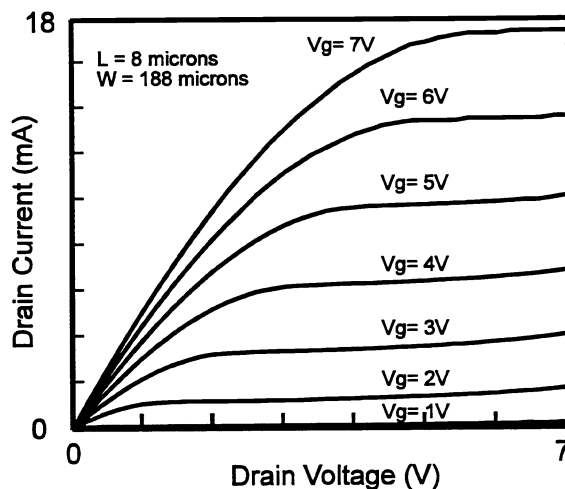


Figure 6. Output Characteristics for n-Channel UTSOS Device

In analyzing the cost of the display, one must consider the cost of: the starting material, the processing of the circuitry, and the assembly of the final package. Four inch diameter SOS wafers are available from Union Carbide for about \$200. Four inch diameter ISE wafers can be purchased from Kopin for about \$500. Since both processes utilize standard silicon processing

equipment, and have roughly the same complexity, we estimate the cost to build the circuits would be about the same. We do not have an estimate for the cost of transferring the ISE circuitry to the glass substrate, but this is an added step which UTSOS does not require. The transfer step will be especially costly if the yield is low. The final assembly costs would be the same. We would therefore expect UTSOS to provide superior performance to ISE at a comparable if not lower cost.

## 5. CONCLUSION

Improvements obtained using UTSOS offer a viable alternative for AMLCD systems. Predicted aperture ratios and pixel sizes are applicable for efficient, small-size, high-density displays with integrated drive and signal processing circuitry.

As the FLC and silicon-based VLSI technologies evolve, benefits will accrue to FLC/UTSOS devices at comparatively modest development cost. Specifically, the silicon-based VLSI industry's continuing drive toward smaller and smaller feature sizes will result in the capability to make devices with smaller and smaller pixels. No other technology will eclipse silicon-based VLSI in this regard for the foreseeable future. The ability to take advantage of such commercially-driven technology development is a compelling argument in favor of our approach. It is now resulting in high-performance devices, and will show continued evolutionary improvement at modest cost into the future. Competing single-crystal technologies using ISE and transfer techniques are not expected to provide a lower cost when one considers the full fabrication cost of the display.

## 6. ACKNOWLEDGEMENTS

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