Invited Paper

256x256 FERROELECTRIC LIQUID CRYSTAL SPATIAL LIGHT MODULATOR

David B. Banas*, Mark A. Handschy, Charles Crandall

Displaytech, Inc., 2602 Clover Basin Dr., Longmont, CO 80503

ABSTRACT

We present a binary reflective spatial light modulator (SLM) constructed using a patented ferroelectric liquid crystal (FLC) technique. The device is built atop a planarized 0.6 μm CMOS SRAM backplane with 15 μm pixel pitch and 88% fill factor. The device achieves better than 25% optical throughput when used with collimated laser light and better than 100:1 contrast when oriented for amplitude modulation. When oriented for phase modulation, the device achieves 180 degrees of phase shift between its 2 states. The device can be operated as fast as 5kHz with complete switching of the liquid crystal. Applications in the fields of optical computing and optical information processing are suggested.

Keywords: FLC, SLM, photonics, optical computing, optical information processing, correlator, display

1. INTRODUCTION TO FLC DEVICE PHYSICS

The basic operating principles of reflective FLC devices are as follows. A thin layer of FLC material is sandwiched between a metal conductor and a glass window coated with a transparent conductive layer such as indium tin oxide (ITO). A voltage is then applied across the FLC layer and, depending on the polarity of the applied voltage, the fast axis of the FLC material, which is birefringent, is forced into one of two possible states. The vector describing the fast axis orientation is perpendicular to the conductive surface normal in both possible orientations with the 2 orientations separated from one another by an angle of approximately 45 degrees. Thus, when viewed along the conductive surface normal, the device can be thought of as a waveplate with an electrically switchable fast axis orientation. In order to understand the effects of the reflective nature of the device, we model the device using Jones matrices. The Jones matrix representing a transmissive waveplate of arbitrary retardance and orientation is[1]:

$$T(\theta,\varphi)=\begin{bmatrix}\cos^2\theta\cdot e^{i\varphi/2}+\sin^2\theta\cdot e^{-i\varphi/2} & \cos\theta\cdot\sin\theta\cdot\left(e^{i\varphi/2}-e^{-i\varphi/2}\right)\\ \cos\theta\cdot\sin\theta\cdot\left(e^{i\varphi/2}-e^{-i\varphi/2}\right) & \sin^2\theta\cdot e^{i\varphi/2}+\cos^2\theta\cdot e^{-i\varphi/2}\end{bmatrix}, \tag{1}$$

where θ is the angle between the fast axis orientation vector and the x-axis and ϕ is the phase retardance of the plate. Note that the incident light is assumed to be coherent, and propagating along the z-axis. It now remains to be shown that a reflective device with retardance, $\phi/2$ (after one pass), is mathematically equivalent to a transmissive device with retardance, ϕ. The situation is expressed mathematically below.

$$R(\theta,\varphi/2)=T(-\theta,\varphi/2)\cdot\begin{bmatrix}-1 & 0\\ 0 & 1\end{bmatrix}\cdot T(\theta,\varphi/2), \tag{2}$$

where the matrix in Eq. (2) represents the reflective metal conductor. Carrying out the matrix multiplications on the right side of Eq. (2), we find that:

$$R(\theta,\varphi/2)=\begin{bmatrix}-1 & 0\\ 0 & 1\end{bmatrix}\cdot T(\theta,\varphi), \tag{3}$$

Therefore, except for a 180 degree rotation about the y-axis (caused by reflection off the metal conductor), a reflective device with retardance, ϕ/2 (after one pass), is equivalent to a transmissive device with retardance, ϕ.

2. BASIC AMPLITUDE MODULATION SYSTEM CONFIGURATION

The simplest amplitude modulating system, using a reflective FLC cell, is formed by placing a linear polarizer over the glass window of the FLC cell such that its transmission axis is parallel to the fast axis of the FLC cell in one of its 2 possible states. The thickness of the FLC cell is such that, at the wavelength of interest, the cell acts as a half-wave plate. The configuration is show below.

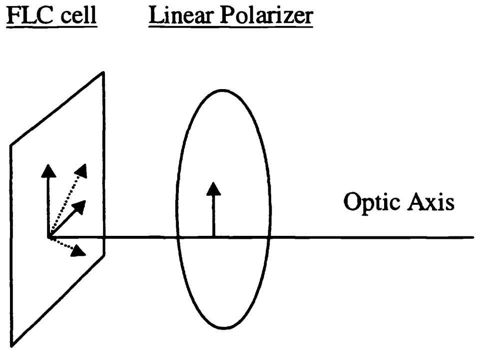

Figure 1 - Basic Amplitude Modulation System Configuration

In the figure above, one possible orientation of the FLC material is shown as 2 solid arrows while the other possible orientation is shown as 2 dashed arrows. In both cases the longer of the 2 arrows represents the fast axis. The transmission axis of the linear polarizer is shown as 1 solid vertical arrow. In this configuration the "on" state is that in which the fast axis of the FLC material is parallel to the transmission axis of the linear polarizer (solid arrows). In this state the incident light is unchanged by the FLC cell and, thus, passed by the polarizer upon reflection. When the FLC material is electrically switched into the other state (dashed arrows), the polarization vector of the incident light is rotated 90 degrees upon reflection from the FLC cell and is blocked by the polarizer, thus constituting the "off" state. Contrast ratios using this arrangement are usually quite poor owing to the fact that any deviation in the FLC cell from exact half-wave retardance results in elliptically polarized light upon reflection in the "off" state, the vertical component of which is passed by the polarizer. Much better contrast ratios can be achieved by a system configuration in which the "off" state corresponds to the FLC cell state which leaves the light unchanged. This configuration is described next.

3. HIGH CONTRAST AMPLITUDE MODULATION SYSTEM CONFIGURATION

Figure 2, below, shows a system configuration for amplitude modulation which achieves much better contrast ratios than the system described above. In this configuration 2 polarizers are used, one to polarize the incoming light and the other to analyze the outgoing light. The beamsplitter is necessary in order to separate the input and output beams. The analyzer is set crossed to the polarizer so that the "off" state of the system corresponds to the FLC device state in which the light is unchanged upon passing through the FLC cell. In this state the fast axis is parallel to the incident light's polarization vector and the light reflects off the FLC device unchanged and is, thus, blocked by the analyzer. When the FLC material is electrically switched into the other state, the polarization vector of the incident light is rotated 90 degrees upon passing through the FLC cell and is passed by the analyzer thus constituting the "on" state. In this configuration the system's contrast ratio is limited, theoretically, only by the extinction ratio of the polarizers used. However, in practice, inconsistencies in the FLC material alignment are the limiting factor.

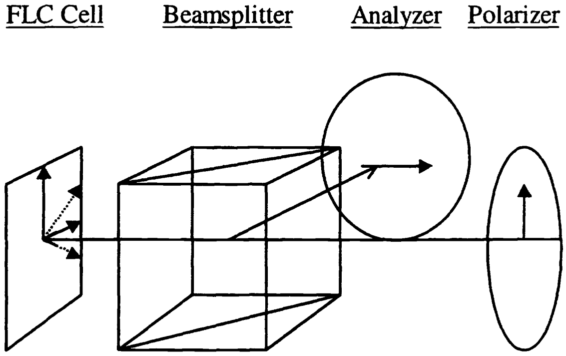

Figure 2 – High Contrast Amplitude Modulation System Configuration

4. PHASE MODULATION SYSTEM CONFIGURATION

Figure 3, below, shows a system configuration in which the FLC device is used to modulate the phase of the incident light. In this configuration the FLC device is oriented such that the incident light's polarization vector bisects the angle formed by the 2 possible fast axis orientations. In one fast axis orientation the polarization vector of the incident light is rotated 45 degrees clockwise upon passing through the FLC cell and, in the other fast axis orientation, the vector is rotated 45 degrees counterclockwise. Upon passing through the analyzer, both states produce light polarized along the horizontal axis, 180 degrees out of phase with eachother. This particular system configuration can be used for performing Binary Phase Only Modulation (BPOM) which is very useful when using the SLM to construct a correlator.

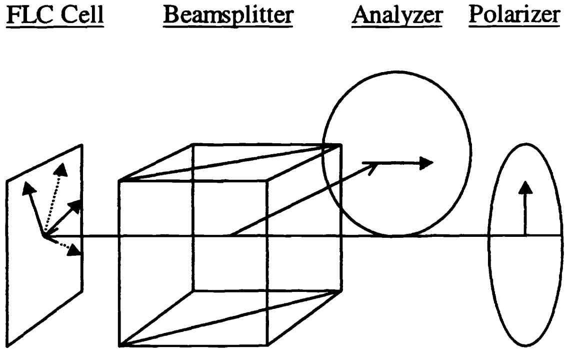

Figure 3 - Phase Modulation System Configuration

5. SLM DEVICE DESCRIPTION

Figure 4, below, shows the various components of a complete reflective FLC SLM.

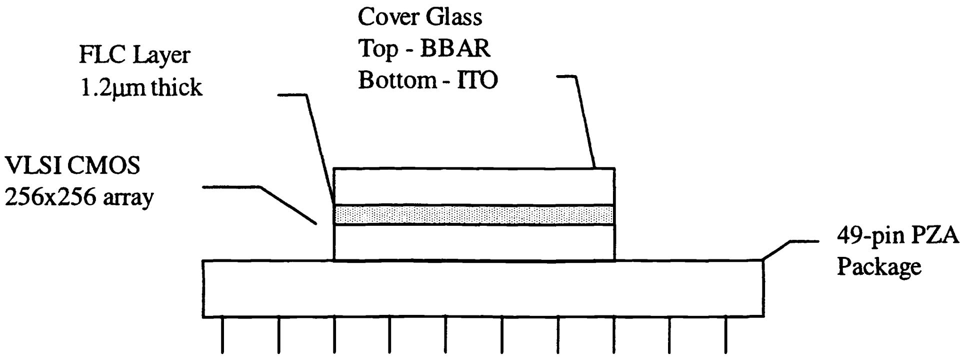

Figure 4 - SLM Cross Section

5.1 CMOS SRAM backplane

The heart of the device is the silicon backplane which is manufactured using standard 0.6 & 0.8 μm CMOS processes. The active area of this silicon die consists of 3 major areas as shown in figure 5 below. The main area is the pixelated array which consists of 65,536 individually addressable standard SRAM cells arranged in a 256x256 square array. The "fill factor" of this array, defined as the ratio of the area covered with metal to the total area of the array, is 87%. Outside this pixelated area is the "apron" region which is a square contiguous ring of metal connected to a single package pin. This area can be used for border definition by driving it opposite to the background region of the image being shown in the pixelated area. Within the apron region are several "fiducial" pixels which are electrically connected but driven independently of the apron via a separate package pin. These fiducial pixels can be driven in contrast to the apron and used for device alignment in critical applications.

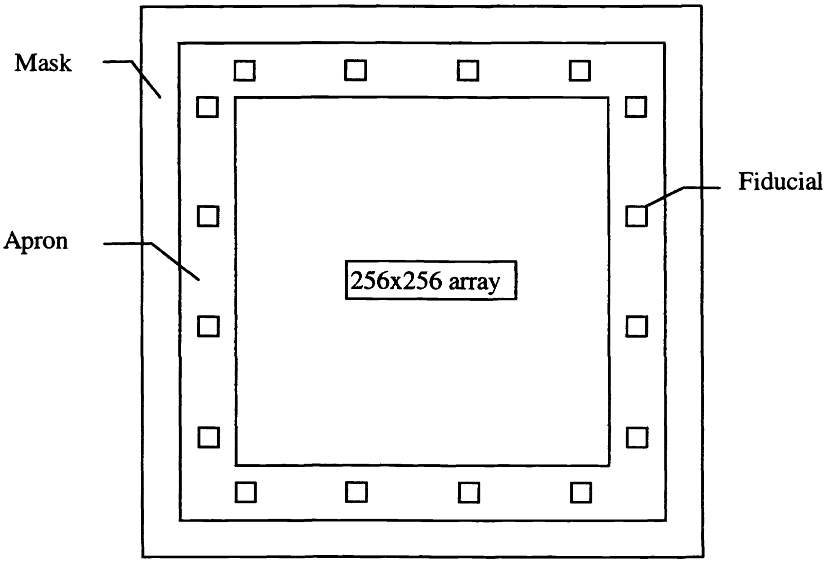

Figure 5 - SLM CMOS Plan View

The silicon dice used for SLM manufacture are subject to a Chemical-Mechanical Polishing (CMP) process at the foundry prior to delivery to Displaytech. This process drastically improves the planarization of the raw dice over that achieved with ordinary CMOS processes. This increased die planarization leads directly to increased optical throughput by reducing the diffraction which occurs with non-planar topologies. Typical device throughput, using a planarized die, is 40% (This means that 40% of the incident light is reflected back into the diffractive 0th order.) while that using an ordinary die is less than 10%.

5.2 Window assembly / FLC fill

A planarized silicon die becomes a SLM only after the patent-protected manufacturing step known as "window assembly/FLC fill" has been completed. In this manufacturing step a glass window, coated on the underside with ITO, is secured atop the silicon die using thickness-controlled adhesive, producing a gap thickness of approximately 1μm. The gap thickness is variable so that the device may be tuned to different wavelengths. Prior to assembly, the underside of the window is coated with a special alignment material using a proprietary process. The purpose of this material is to keep the FLC molecules well aligned in the finished device. (Recall from the discussion above that the factor which limits device contrast is FLC alignment.) A void is left in the otherwise continuous ring of adhesive through which the gap may be filled with FLC material. Once the adhesive has cured, the gap is filled with FLC material via capillary action. The fill hole is then sealed to prevent seepage of the FLC material

5.3 Packaging

The final step in the manufacture of a SLM is the packaging of the assembled and filled die. The package constitutes the physical and electrical interface between the SLM and the outside world.

5.3.1 Physical description

The package currently used for SLM manufacture was custom engineered for Displaytech and is referred to as a "49-pin Pin Zigzag Array (PZA)". The package combines 2, 5x5, 0.1" center-to-center pin arrays in a staggered interstitial arrangement in order to provide the large pin count needed in as small an area as possible. Figure 6, below, contains a photograph of the SLM mounted in a 49-pin PZA package. As can be seen in the figure, the entire package occupies an area roughly 0.5" square while providing the pin count necessary to support a 32-bit data bus as well as all control signals required by the SLM.

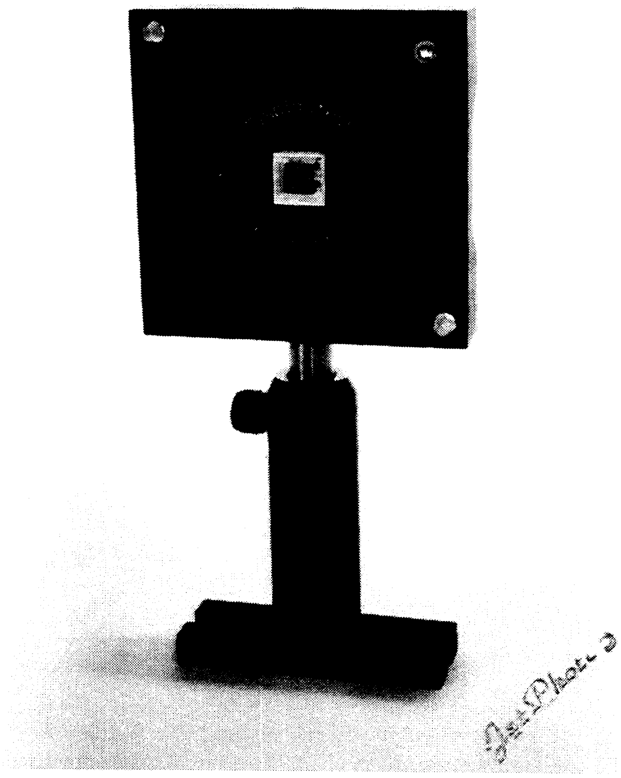

Figure 6 - Photograph of SLM in 49-pin PZA package

5.3.2 Electrical interface

The electrical interface to the SLM consists of a 32-bit data bus, 4 control signals, and 3 direct-drive fiducial controls. The SLM accepts data in 32-bit words at a maximum rate of 80MHz (40MHz using current driver). This correlates to a total minimum SLM writing time of 25.6µs (51.2µs using current driver). The SLM has an internal address counter which is incremented every time a data word is clocked in through the data bus so that external addressing is unnecessary. This helps greatly reduce the required pin count. However, external addressing is possible if desired. The 4 control signals used by the SLM are:

- Reset - resets the internal address counter to word #0
- Clock - clocks the data in and increments the internal address counter
- Invert - controls on-board data inversion (useful for maintaining d.c. balance condition)
- Blank - sets all pixels to same state (used for "parking" the SLM when not used for an extended time)

The remaining 3 signals are used to directly drive the 3 fiducial areas of the chip. Two of these areas, the apron and the fiducial pixels, were described above. The third, called the "mask", is just all the remaining metal outside the apron.

5.3.3 Phase/amplitude modulators

The packaged SLMs are sold in 2 configurations: phase and amplitude modulators. The only difference between the 2 configurations is the orientation of the fast axis of the FLC material relative to the edge of the pixelated array. For instance, a phase modulator can easily become an amplitude modulator if the user doesn't mind rotating the device 22.5 degrees. However, sometimes this rotation is inconvenient, so both configurations are manufactured by Displaytech.

6. SLM DEVICE CHARACTERISTICS

In this section we describe the measurements made at Displaytech for the purpose of characterizing SLMs. The experimental techniques used are described and data is reported which reveals the actual operating characteristics of the Displaytech SLM.

6.1 Device response times

SLM response time can be divided into 2 categories: electrical write time and FLC rise/fall time. These 2 factors, together with the need to provide d.c. balance across the FLC layer, define the maximum useable frame rate of the device.

6.1.1 Electrical write time

The time required to electrically write the SLM with one full frame's worth of data is governed, theoretically, by the number of pixels on the SLM, the width of the data bus, and the maximum clock speed at which data can be reliably clocked in to the SLM. Currently, the SLM contains 65,536 pixels, uses a 32-bit wide data bus, and can be clocked at a maximum speed of 80MHz. This yields a minimum possible electrical write time of 25.6μs. In practice, the minimum electrical write time is limited by the drive electronics. The SLM driver currently manufactured by Displaytech is capable of writing a full frame of data to the SLM in just over 100μs.

6.1.2 FLC response time

The time required for the FLC material to respond to the newly written electrical data is a function of the FLC material itself, the gap thickness of the SLM, and the operating voltage of the SLM. Current devices manufactured with a gap thickness of approximately 1μm (tuned for 690 nm operation), using the most recently available materials, and operating from a standard 5 volt logic supply achieve response times of approximately 150μs. The histogram in figure 7, below, shows the spread in measured response times for all SLMs on which we have data.

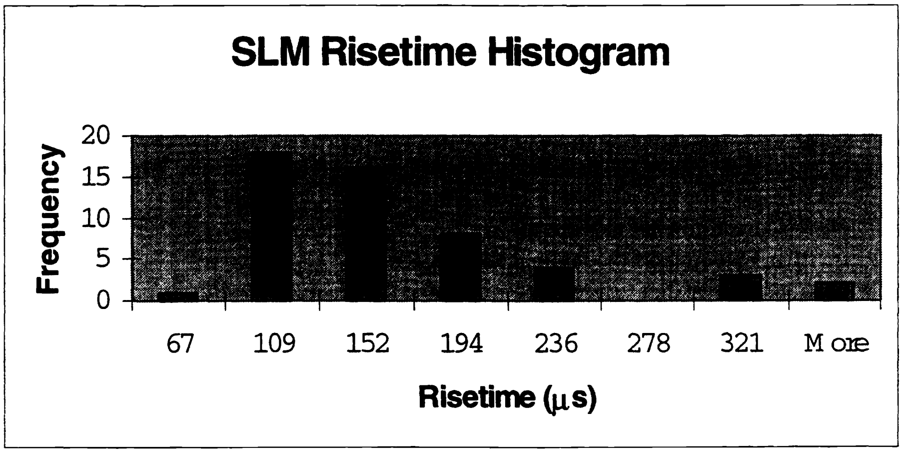

Figure 7 - Histogram of SLM response times

6.1.3 Maximum useable frame rate

Summing the electrical write time (25.6μs) and the FLC response time (150μs) and adding some time for the image to be used before being overwritten yields a maximum useable frame rate of approximately 5kHz. However, in order to maintain a d.c. balance condition across the FLC layer, the user must write the inverse of every image written to the SLM for an equal amount of time. This has the effect of reducing the maximum useable frame rate by a factor of 2.

6.2 Device contrast

When the SLM is operated as an amplitude modulator, its contrast ratio is a meaningful indicator of its quality. Contrast ratio is defined as the ratio of the intensity of the light transmitted through the system (SLM and polarizing optics) in the "on" state to that transmitted in the "off" state when the device has been oriented for best extinction in the "off" state. The histogram in figure 8, below, shows the spread in measured contrast ratios for all SLMs on which we have data.

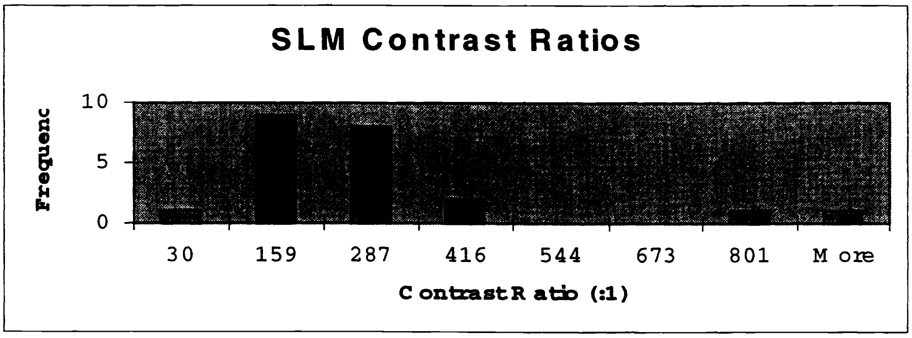

Figure 8 - Histogram of SLM Contrast Ratios

6.3 Device throughput

One of the most important SLM characteristics of concern to the optical computing community is optical efficiency or throughput. Optical efficiency is defined as the percentage of the incident light intensity which is reflected into the diffractive 0th-order of the far-field diffraction pattern when the SLM is operating as an amplitude modulator in the "on" state and has been oriented to give best extinction in the "off" state (oriented for best contrast). Care is taken to adjust the beam spot size at the SLM so as to insure that the beam spot is entirely contained within the pixelated area of the SLM. If this were not done, optical efficiency measurements would be falsely inflated by the d.c. contributions of the fiducial areas of the SLM which have a higher fill factor than the pixelated array.

6.3.1 Theoretical maximum throughput

In judging the relative merit of optical efficiency measurements taken from real SLMs, it is useful to know the theoretically predicted value. This value is found by taking the 2-D Fourier transform, at d.c., of a somewhat idealized model of the SLM's pixelated area. This model assumes perfectly planar pixels, perfect FLC alignment, and perfect half-wave retardance. Furthermore, the model assumes that the contribution to the 0th-order spot made by the area between pixels is identically 0. The 2-D Fourier transform is given by,

$$S(u,v)=\iint s(x,y)e^{-i2\pi(ux+vy)}dxdy, \tag{4}$$

where s(x,y) is the SLM model function described above and the double integral is taken over one pixel period in both directions. Evaluating the above equation at d.c. (u=v=0) and implementing the assumptions of the model, we find, for the expected amplitude in the d.c. spot of the far-field diffraction pattern,

$$S(0,0)=\iint_{0:\alpha} dxdy=\alpha^2, \tag{5}$$

where α^2 is the fill factor of the pixelated area of the SLM which, for the current generation of SLMs, is 87%. The expected intensity at the d.c. spot will be the square of the expected amplitude, or, α^4. Therefore, we find that the theoretically predicted optical efficiency is just the square of the SLM's fill factor or, for the current generation of SLMs, 75.7%.

6.3.2 Measured throughput

The histogram in figure 9, below, shows the spread in measured optical throughput for all SLMs on which we have data.

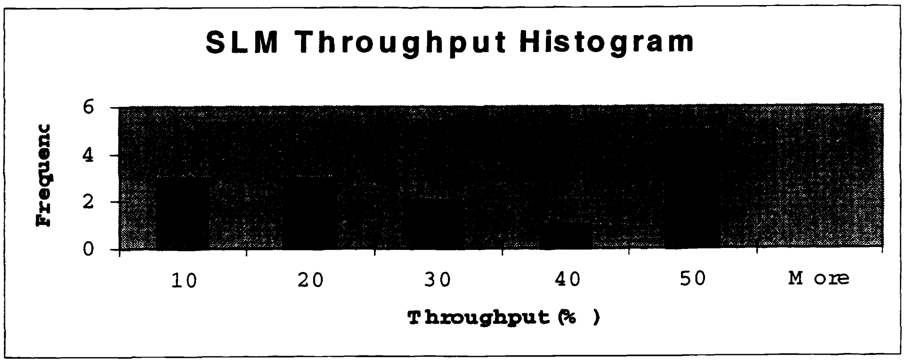

Figure 9 - Histogram of SLM Throughput Values

6.4 Spatial uniformity

All of the measurements described above are "global" in the sense that they measure the whole SLM at once, averaging the behavior of individual pixels into one gross measurement. It is of interest, however, to know what sort of spatial uniformity exists within the pixelated area of the SLM. Currently, Displaytech is working towards incorporating various spatial uniformity tests into the standard suite of quality assurance measurements. However, as this work was begun quite recently, no data were available for this paper. Here we describe the issues and outline our intended measurement techniques.

6.4.1 Alignment uniformity

The most critical spatial uniformity issue is that of FLC alignment since, as explained previously, it is the limiting factor to device contrast. Visually, alignment non-uniformities are fairly easy to detect since they reduce the contrast of the device. A typical visual inspection for alignment uniformity is conducted as follows. The device is programmed to alternately display an "all on" and an "all off" pattern and oriented to give best contrast at its center while being observed through an imaging microscope. The contrast at the device extremities is then observed and, if the device must be rotated to achieve best contrast at the extremities, it contains alignment non-uniformities. The amount of rotation necessary to achieve best extinction at the extremities of the device is a direct quantitative measure of the amount of alignment non-uniformity in the device.

6.4.2 Gap thickness uniformity

Also of interest is the spatial uniformity of the gap thickness, as variations in this value will correspond to variations in retardance across the device. As with alignment uniformity, there is a visual inspection procedure already in place at Displaytech for filtering out grossly errant devices. In this case also, the device is observed through an imaging microscope and programmed to alternately display “all on” and “all off” patterns. However, the critical observation in this case is made during the “all on” phase of operation. A device with significant gap thickness variation across its clear aperture will exhibit colored fringes, when observed in white light, reminiscent of a rainbow. This occurs because the varying gap thickness “tunes” different areas of the device for peak transmittance at varying wavelengths within the visible spectrum. The spatial frequency of color variation on such a device is a direct quantitative measure of the degree of non-uniformity in its gap thickness.

6.4.3 Reflected wavefront flatness

Lastly, it is of interest to know the overall flatness of the wavefront being reflected by the device. If the phase of this wavefront is distorted or discontinuous it will render the device unusable for phase-sensitive optical processing applications such as correlation. Displaytech uses the industry standard method of interferometric observation in order to characterize the nature of the wavefront reflected by our devices.

7. SLM DEVICE APPLICATIONS

The fields of optical computing, optical information processing, and optical signal processing are rich with opportunity for new and clever applications which take specific advantage of the key features of Displaytech’s SLM. A few key applications of the SLM are described below.

7.1 Miniature optical correlator

Figure 10, below, shows the layout of a Vanderlugt 4f optical correlator[2] built around the Displaytech SLM. The compact size of the correlator (approximately 7” in length) is directly attributable to the short characteristic length (approximately 88mm in the red) of the Displaytech SLM.

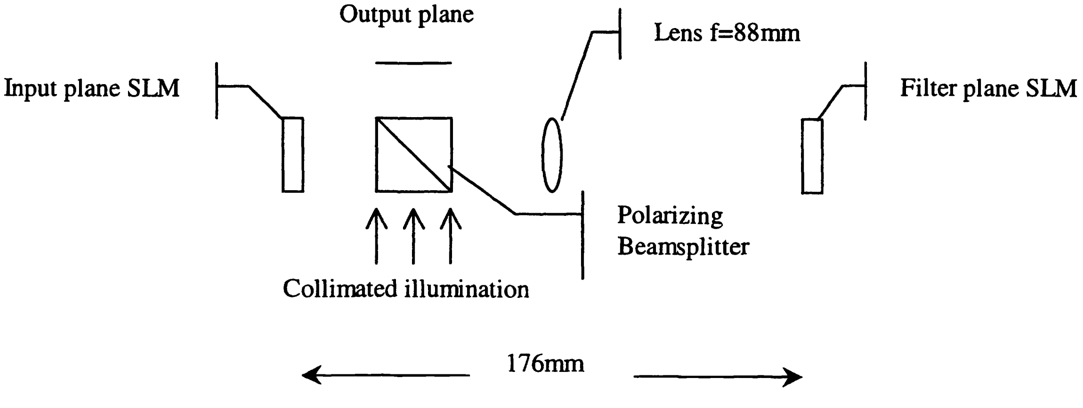

Figure 10 - Miniature optical correlator using Displaytech SLM

Possible applications of this miniature optical correlator include target identification/tracking, machine vision inspection, finger print identification, and optical character/word recognition.

7.2 Other SLM applications

Other optical processing applications which stand to make good use of the unique features of Displaytech's SLM include:

- Holographic storage
- Electronic film printing

CONCLUSION

We have described a 256x256 active backplane SLM which is constructed atop planarized CMOS SRAM circuitry and capable of amplitude or phase modulation of the incident light at a frame rate of 5kHz. We have described the real-world quality assurance issues associated with high volume manufacture of such devices and the inspection/measurement techniques being used to address those issues. Also, we have outlined our intended improvements to those techniques so as to address the various spatial uniformity issues associated with SLM device quality. Finally, we have given an example of a miniature optical correlator which takes advantage of the short characteristic length of our device and have suggested other applications in the various optical processing fields which might make use of our device's unique features.

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NASA Johnson Space Center
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